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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CHEN, JACK S J

ART UNIT	PAPER NUMBER
2813	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/052,853	Applicant(s) Wada et al.
	Examiner Jack Chen	Art Unit 2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Sep 12, 2002 .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 9-15 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 9-15 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on Nov 9, 2001 is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. In response to the communications dated September 12, 2002, claims 9-15 are active in this application.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, *the passivation layer covering the flash memory cell* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9-15 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Re claim 9, the phrase "the passivation layer covering the flash memory cell" is not supported by the original disclosure.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9-11, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiyohiko [JPO Publication Number: 04-078,173].

Kiyohiko discloses a flash memory (called "EPROM" in Kiyohiko, English abstract section, lines 1-4) comprising: a semiconductor substrate 1 (fig. 1) that includes a flash memory cell (called "EPROM element" in Kiyohiko, English abstract section, lines 1-4) that has a floating gate 3 (fig. 1, English abstract section, lines 10); a conductive layer 7 (fig. 1, called "aluminum wiring" in Kiyohiko, English abstract section, line 8) formed on the substrate 1; and a passivation layer 9 and 10 (fig. 1, English abstract section, lines 5-6) formed on the conductive layer 7 that is not transparent to ultraviolet light (called "opaque to ultraviolet rays" in Kiyohiko, English

abstract section, line 9), the passivation layer covering the flash memory cell (fig. 1, abstraction section, lines 11-13; note: the passivation layer 9 by itself is covering the flash memory cell, and the passivation layer 10 by itself is also at least covering a least a portion of the flash memory cell).

Regarding claim 10, wherein the passivation layer comprises a barrier layer 9 (fig. 1, called "silicon nitride film" in Kiyohiko, English abstract section, line 5, which is the same material as applicant's disclosure, see page 5, line 4 of the instant application) and a stress reduction layer 10 (fig. 1, called "polyimide film" in Kiyohiko, English abstract section, lines 5-6 and 2-4, which is the same material as applicant's disclosure, see page 5, lines 4-5 of the instant application).

Regarding claim 11, wherein the passivation layer comprises a silicon nitride layer 9 (fig. 1, called "silicon nitride film" in Kiyohiko, English abstract section, line 5) and a polyimide layer 10 (fig. 1, called "polyimide film" in Kiyohiko, English abstract section, lines 5-6 and 2-4).

Regarding claim 15, wherein the passivation layer comprises a polyimide layer 10 (fig. 1, called "polyimide film" in Kiyohiko, English abstract section, lines 5-6 and 2-4).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyohiko [JPO Publication Number: 04-078,173] in view of Jeuch [U.S. Patent Number: 5,138,573].

Kiyohiko disclosed above in paragraph 6, in particular, the device comprises a floating gate 3 having the physical gate length as shown in fig. 1; however, Kiyohiko is silent to the floating gate having a length that is less than about 0.5 microns.

Jeuch teaches a EPROM (col. 1, lines 5-10) comprising a floating gate (col. 2, lines 49-53) having a length (called "width" in Jeuch, col. 2, lines 49-50) that is less than 0.5 microns (col. 2, lines 49-53 and col. 3, lines 44-50), which greatly contributes to reducing the dimensions of the storage cell (col. 2, lines 49-53).

Regarding claim 13, Kiyohiko shows the conductive layer forms the final metal interconnect 7 (fig. 1, called "aluminum wiring" in Kiyohiko, English abstract section, line 8) for

the flash memory (called "EPROM" in Kiyohiko, English abstract section, lines 1-4), upon which is formed the passivation layer 9 and 10 (fig. 1).

Regarding claim 14, Kiyohiko shows the silicon nitride layer 9 (fig. 1) is about 0.3 μm (page 466, left column, lines 1-3, which corresponds to *3000 angstroms*) thick.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kiyohiko to select the suitable floating gate length as taught by Jeuch in order to reduce the dimensions of the storage cell (col. 2, lines 49-53), such will reduce the dimensions of the integrated circuits and increase the integration density (col. 1, lines 27-30). Further in this regard, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

9. Applicant's arguments filed September 12, 2002 have been fully considered but they are not persuasive.

Applicant stated that the support for the new added limitation (Re claim 9, the phrase "the passivation layer covering the flash memory cell") in claim 9 can be found at page 6, line 3 through page 7, line 2. The Examiner disagrees because page 6, line 3 through page 7, line 2 does not show this particular limitation.

Applicant argued that EPROM and flash memories are different types of memory device. The Examiner disagrees because EPROM is a type of flash memories (flash memories, such as EPROM is non-volatile memory device). Further in this regard, applicant also stated that EPROM is an example of flash memory devices in the specification, page 2, lines 12-16. Furthermore, Kiyohiko teaches a *semiconductor device*, such as *memory transistor* (*EPROM* element).

Applicant further stated that the prior art (Jeuch, U.S./5,138,573) distinguishes EPROMs from flash memories at column 1, lines 6-11. The Examiner disagrees because Jeuch states "More specifically, the invention relates to *EPROM* (Erasable Programmable Read Only Memory) and *EEPROM* (Electrically Erasable Programmable Read Only Memory) cells of ***the flash type***" (which EPROM is a type of flash memory, also see col. 2, lines 4-7).

Applicant stated that the prior art (Kiyohiko) must include the window 11. The Examiner disagrees because the abstract section (lines 11-13), clearly states "*It is not necessary* to provide the window 11 to each EPROM element".

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday (alternate Monday off) from 8:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703)308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen

JACK CHEN
PATENT EXAMINER

November 22, 2002

CARL WHITEHEAD, JR.
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